IN THE CLAIMS

Please amend the claims as follows:

1. -9. (Cancelled)

10. (Previously Presented) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs, wherein said logic circuit is arranged to generate a first binary output as an elementary symmetric function of the binary inputs using exclusive OR logic for combining a plurality of sets of one or more binary inputs, and to generate an N^{th} binary output as an elementary symmetric function of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs.

11. (Previously Presented) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs, wherein said logic circuit is arranged to generate two possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary symmetric functions of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs where N is the number of binary outputs, the sets used for each possible binary output being of two different sizes which are a function of the binary output being generated; and said logic circuit include selector logic to select one of the possible binary outputs based on a more significant binary output value.

12. (Original) A parallel counter according to claim 11, wherein said logic circuit is arranged to generate the two possible binary outputs for the $(N-1)^{th}$ binary output less significant than the N^{th} binary output, as elementary symmetric functions of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively and said selector logic being arranged to select one of the possible binary outputs based on the N^{th} binary output value.

13. (Previously Presented) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs, wherein said logic circuit is arranged to generate two possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary symmetric functions of the binary inputs; and said logic circuit includes selector logic to select one of the possible binary outputs based on a more significant binary output value.

14. (Previously Presented) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs, wherein said logic circuit includes logic units for generating intermediate outputs as elementary symmetric functions of the binary inputs and is arranged to generate a binary output less significant than the N^{th} binary output by combining intermediate outputs of the logic units by AND combining at least the intermediate output of one logic unit

and an inverted output of another logic unit and OR combining the result of the AND combining with another intermediate output.

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15. (Original) A parallel counter according to claim 14, wherein said logic circuit is arranged to generate the k^{th} binary output S_k, where k=0 to t-1 and t is the number of outputs in accordance with the relationship:

$$S_k = \{OR\_n\_2^k \wedge \neg OR\_n\_2^{k+1}\} \vee \{OR\_n\_2^{k+1} + 2^k \wedge \neg OR\_n\_2^{k+2}\}$$
$$\vee \{OR\_n\_2^{k+2} + 2^k \wedge \neg OR\_n\_2^{k+2} + 2^{k+1}\}$$
$$\ldots\ldots\ldots\ldots\ldots\ldots$$
$$\vee OR\_n\_2^t + 2^{t-1} + 2^{t-2} + 2^k$$

where $\wedge$ is the logical AND operation, $\vee$ is the logical OR operation, and $\neg$ is an inversion operation.

16. (Previously Presented) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs, wherein said logic circuit includes a plurality of subcircuit logic modules each generating intermediate binary outputs as an elementary symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

17. (Original) A parallel counter according to claim 16, wherein said subcircuit logic modules are arranged to use OR logic for combining sets of said some of said binary inputs.

18. (Original) A parallel counter according to claim 17, wherein said logic circuit includes one or more logic modules each for generating a binary output as an elementary symmetric function

of the binary inputs using executive OR logic for combining a plurality of sets of one or more binary inputs.

19. (Previously Presented) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs, wherein said logic circuit implements a large elementary symmetric function by implementing a plurality of small elementary symmetric functions and combining the results.

20. (Previously Presented) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs, wherein said logic circuit is divided into a plurality of logic units, each logic unit is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to the logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said logic units, and the binary outputs of said plurality of outputs are generated using binary outputs of a plurality of said logic units.

21. (Currently Amended) A parallel counter according to claim 20, wherein the logic units are arranged hierarchically such that logic units at a higher level in the hierarchy include the logic of at least one logic unit at a lower level in the hierarchy and have more of the binary inputs as inputs than the logic units at a lower level in the hierarchy.

22. (Original) A parallel counter according to claim 20, wherein the binary inputs of said plurality of inputs are divided according to a binary tree into inputs into a plurality of said logic units.

23. (Original) A parallel counter according to claim 22, wherein said logic units are arranged to receive 2^n of said binary inputs, where n is an integer indicating the level of the logic units in the binary tree, said logic circuit has m logic units at each level, where m is a rounded up integer determined from (the number of binary inputs)/ 2^n, logic units having a higher level in the binary tree comprise logic of logic units at lower levels in the binary tree, and each logic unit is arranged to generate logic unit binary outputs as a symmetric function of the binary inputs to the logic unit.

24. (Original) A parallel counter according to claim 23, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as a small elementary symmetric function of the binary inputs to said logic circuit.

25. (Original) A parallel counter according to claim 23, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit using OR logic for combining the binary inputs.

26. (Original) A parallel counter according to claim 25, wherein each logic unit at the first level is arranged to logically AND each of the binary inputs to the logic unit and to logically OR each of the binary inputs to the logic unit to generate the logic unit binary outputs.

27. (Original) A parallel counter according to claim 24, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit using exclusive OR logic for combining the binary inputs.

28. (Original) A parallel counter according to claim 27, wherein each logic unit at the first level is arranged to logically AND each of the binary inputs to the logic unit and to logically

exclusively OR each of the binary inputs to the logic unit to generate the logic unit binary outputs.

29. (Original) A parallel counter according to claim 23, wherein elementary logic units are provided as the logic units at the first level for performing elementary symmetric functions, outputs from each of two primary elementary logic units receiving four logically adjacent binary inputs from said plurality of inputs are input to two secondary elementary logic units, an output from each of the secondary elementary logic units is input to a tertiary elementary logic unit, and said primary, secondary and tertiary elementary logic units form a secondary logic unit at a second level of the binary tree having a binary output comprising a binary output from each of said secondary elementary logic units and two binary outputs from said tertiary elementary logic unit.

30. (Original) A parallel counter according to claim 29, wherein tertiary logic units at a third level of the binary tree each comprise two secondary logic units receiving eight logically adjacent binary inputs from said plurality of inputs, four elementary logic units receiving as inputs the outputs of said two secondary logic units, and further logic for generating binary outputs as a symmetric function of the binary inputs to said tertiary logic unit using the binary outputs of said four elementary logic units.

31. (Previously Presented) A parallel counter according to claim 30, wherein quaternary logic units at a fourth level of the binary tree each comprise two tertiary logic units receiving sixteen logically adjacent binary inputs from said plurality of inputs, four elementary logic units receiving as inputs the outputs of said two tertiary logic units, and further logic for generating binary outputs as a symmetric function of the binary inputs to said quaternary logic unit using the binary outputs of said four elementary logic units.

32. (Original) A parallel counter according to claim 23, wherein elementary logic units are provided as the logic units at the first level for performing elementary symmetric functions, and logic units for higher levels are comprised of logic units of lower levels.

33. (Original) A parallel counter according to claim 32, wherein said logic units for higher levels above the second level comprise logic units of an immediately preceding level and elementary logic units.

34. (Original) A parallel counter according to claim 23, wherein each logic unit at each level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit using OR logic for combining the binary inputs.

35. (Original) A parallel counter according to claim 23, wherein each logic unit at each level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit using exclusive OR logic for combining the binary inputs.

36. (Original) A parallel counter according to claim 20, wherein the logic units are arranged hierarchically and at least one logic unit in at least one level of the hierarchy implements an inverted elementary symmetric function.

37. (Original) A parallel counter according to claim 36, wherein logic units at an odd number of levels in the hierarchy implement inverted elementary symmetric functions, logic units at an even number of levels in the hierarchy implement symmetric functions, and the inputs to the logic units at the first level of the hierarchy are inverted.

38. (Original) A parallel counter according to claim 36, wherein logic units at an even number of levels in the hierarchy implement inverted elementary symmetric functions, logic units at an even number of levels in the hierarchy implement symmetric functions, and the inputs to the logic units at the first level of the hierarchy are input to logic units in a first level in the hierarchy uninverted.

39. (Original) A parallel counter according to claim 36, wherein logic units at an even number of levels in the hierarchy implement inverted elementary symmetric functions, logic units at an

odd number of levels in the hierarchy implement symmetric functions, and the inputs to the logic units at the first level of the hierarchy are inverted.

40. (Original) A parallel counter according to claim 36, wherein at least one logic unit in at least one level of the hierarchy implements an elementary symmetric function and the or each inverted elementary symmetric function and the or each elementary symmetric function are implemented in alternated levels in the hierarchy.

41. (Original) A parallel counter according to claim 36, wherein logic units in at least one level in the hierarchy comprise inversion logic.

42. (Original) A parallel counter according to claim 36, wherein the logic units are arranged hierarchically in a binary tree structure.

43. (Previously Presented) A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs, wherein the number of inputs is at least four and the number of outputs is at least three.

44. (Original) A parallel counter comprising:

at least five inputs for receiving a binary number as a plurality of binary inputs;

at least three outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of binary outputs and for generating each of the plurality of binary outputs as an elementary symmetric function of the binary inputs.

45. (Original) A parallel counter according to claim 44, wherein said logic circuit is arranged to generate at least two outputs independently of each other.

46. (Original) A parallel counter comprising:

n inputs for receiving a binary number as binary inputs, where $4 \geq n \geq 7$;

three outputs for outputting binary code indicating the number of binary ones in the binary inputs; and

a logic circuit connected between the inputs and the three outputs and for generating a first output as an elementary symmetric function EXOR_n_1 of the binary inputs, a second output as a combination of three elementary symmetric functions OR_n_2, OR_n_4 and OR_n_6, and a third output as an elementary symmetric function OR_n_4.

47. (Original) A parallel counter comprising:

n inputs for receiving a binary number as binary inputs, where $8 \geq n \geq 15$;

four outputs for outputting binary code indicating the number of binary ones in the binary inputs; and

a logic circuit connected between the inputs and the four outputs and for generating a first output as an elementary symmetric function EXOR_n_1 of the binary inputs, a second output as an elementary symmetric function EXOR_n_2 of the binary inputs, a third output as a combination of three elementary symmetric functions OR_n_4_, OR_n_8 and OR_n_12, and a third output as an elementary symmetric function OR_n_8.

48. – 68. (Canceled)

69. (Previously Presented) A logic circuit comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the or each binary output and for generating the or each binary output in accordance with a threshold function implemented as a binary tree and having a threshold of at least 2;

wherein the logic elements are arranged to generate the or each binary output as an elementary symmetric function of the binary inputs;

wherein the logic elements are arranged to generate at least one of the binary outputs as an OR symmetric function of the binary inputs; and

wherein the logic elements are arranged to generate at least one of the binary outputs as an exclusive OR symmetric function of the binary inputs.

70. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the or each binary output and for generating the or each binary output in accordance with a threshold function implemented as a binary tree and having a threshold of at least 2; and

wherein said logic elements comprise a plurality of subcircuit logic modules each generating intermediate binary outputs as an elementary symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate the or each binary output.

71. (Previously Presented) A logic circuit comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the or each binary output and for generating the or each binary output in accordance with a threshold function implemented as a binary tree and having a threshold of at least 2;

wherein the logic elements are arranged to generate the or each binary output as an elementary symmetric function of the binary inputs; and

wherein said logic elements comprise a plurality of logic modules each for generating intermediate binary outputs as an elementary symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate the or each binary

output, and.the logic modules are arranged hierarchically and at least one logic module in at least one level of the hierarchy implements an inverted elementary symmetric function.

72. (Original) A logic circuit according to claim 71, wherein logic modules at an odd number of levels in the hierarchy implement inverted elementary symmetric functions, logic modules at an even number of levels in the hierarchy implement symmetric functions, and the inputs to the logic modules at the first level of the hierarchy are inverted.

73. (Original) A logic circuit according to claim 71, wherein logic modules at an even number of levels in the hierarchy implement inverted elementary symmetric functions, logic modules at an even number of levels in the hierarchy implement symmetric functions, and the inputs to the logic modules at the first level of the hierarchy are input to logic units in a first level in the hierarchy uninverted.

74. (Original) A logic circuit according to claim 71, wherein logic modules at an even number of levels in the hierarchy implement inverted elementary symmetric functions, logic modules at an odd number of levels in the hierarchy implement symmetric functions, and the inputs to the logic modules at the first level of the hierarchy are inverted.

75. (Original) A logic circuit according to claim 71, wherein at least one logic module in at least one level of the hierarchy implements an elementary symmetric function, and the or each inverted elementary symmetric function and the or each elementary symmetric function are implemented in alternated levels in the hierarchy.

76. (Original) A logic circuit according to claim 71, wherein logic modules in at least one level in the hierarchy comprise inversion logic.

77. (Original) A logic circuit according to claim 71, wherein the logic modules are arranged hierarchically in a binary tree structure.

78. (Cancelled)

79. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the plurality of binary outputs arranged to generate the or each of the plurality of binary outputs as an elementary symmetric function of the binary inputs; and

wherein said logic elements are arranged to generate at least one of the binary outputs as an elementary symmetric function of the binary inputs using exclusive OR logic for combining a plurality of sets of one or more binary inputs.

80. – 86. (Cancelled)

87. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the plurality of binary outputs arranged to generate the or each of the plurality of binary outputs as an elementary symmetric function of the binary inputs; and

wherein said logic elements are arranged to generate a first binary output as an elementary symmetric function of the binary inputs using exclusive OR logic for combining a plurality of sets of one or more binary inputs, and to generate an N^{th} binary output as an elementary symmetric function of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs.

88. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the plurality of binary outputs arranged to generate the or each of the plurality of binary outputs as an elementary symmetric function of the binary inputs; and

wherein said logic elements are arranged to generate two possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary symmetric functions of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs where N is the number of binary outputs, the sets used for each possible binary output being of two different sizes which are a function of the binary output being generated; and said logic elements include selector logic to select one of the possible binary outputs based on a more significant binary output value.

89. (Original) A logic circuit according to claim 88, wherein said logic elements are arranged to generate the two possible binary outputs for the $(N-1)^{th}$ binary output less significant than the N^{th} binary output, as elementary symmetric functions of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively and said selector logic being arranged to select one of the possible binary outputs based on the N^{th} binary output value.

90. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the plurality of binary outputs arranged to generate the or each of the plurality of binary outputs as an elementary symmetric function of the binary inputs; and

wherein said logic elements are arranged to generate two possible binary outputs for a binary output less significant than the N^{th} binary output, as elementary symmetric functions of the binary inputs; and said logic elements include selector logic to select one of the possible binary outputs based on a more significant binary output value.

91. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the plurality of binary outputs arranged to generate the or each of the plurality of binary outputs as an elementary symmetric function of the binary inputs; and

wherein said logic elements include logic units for generating intermediate outputs as elementary symmetric functions of the binary inputs, and are arranged to generate a binary output less significant than the N^{th} binary output by combining intermediate outputs of the logic units by AND combining at least the intermediate output of one logic unit and an inverted output of another logic unit and OR combining the result of the AND combining with another intermediate output.

92. (Original) A logic circuit according to claim 91, wherein said logic elements are arranged to generate the k^{th} binary output S_k, where k=0 to t-1 and t is the number of outputs in accordance with the relationship:

$$S_k = \{OR\_n\_2^k \wedge \neg OR\_n\_2^{k+1}\} \vee \{OR\_n\_2^{k+1} + 2^k \wedge \neg OR\_n\_2^{k+2}\}$$
$$\vee \{OR\_n\_2^{k+2} + 2^k \wedge \neg OR\_n\_2^{k+2} + 2^{k+1}\}$$
$$\ldots\ldots\ldots\ldots\ldots\ldots\ldots$$
$$\vee OR\_n\_2^t + 2^{t-1} + 2^{t-2} + 2^k$$

where $\wedge$ is the logical AND operation, $\vee$ is the logical OR operation, and $\neg$ is an inversion operation.

93. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the plurality of binary outputs arranged to generate the or each of the plurality of binary outputs as an elementary symmetric function of the binary inputs; and

wherein said logic elements include a plurality of subcircuit logic modules each generating intermediate binary outputs as an elementary symmetric function of some of the

binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

94. (Original) A logic circuit according to claim 93, wherein said subcircuit logic modules are arranged to use OR logic for combining sets of said some of said binary inputs.

95. (Original) A logic circuit according to claim 94, wherein said logic elements include one or more logic modules each for generating a binary output as an elementary symmetric function of the binary inputs using executive OR logic for combining a plurality of sets of one or more binary inputs.

96. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the plurality of binary outputs arranged to generate the or each of the plurality of binary outputs as an elementary symmetric function of the binary inputs; and

wherein said logic elements implement a large elementary symmetric function by implementing a plurality of small elementary symmetric functions and combining the results.

97. (Previously Presented) A logic circuit, comprising:

at least four inputs for receiving a binary number as a plurality of binary inputs;

at least one output for outputting binary code;

logic elements connected between the plurality of inputs and the plurality of binary outputs arranged to generate the or each of the plurality of binary outputs as an elementary symmetric function of the binary inputs; and

wherein said logic elements are divided into a plurality of logic units, each logic unit is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to the logic unit, the binary inputs of said plurality of inputs are divided into inputs into a

plurality of said logic units, and the binary outputs of said plurality of outputs are generated using binary outputs of a plurality of said logic units.

98. (Previously Presented) A logic circuit according to claim 97, wherein the logic units are arranged hierarchically such that logic units at a higher level in the hierarchy include the logic of at least one logic unit at a lower level in the hierarchy and have more of the binary inputs as inputs than the logic units at a lower level in the hierarchy.

99. (Original) A logic circuit according to claim 97, wherein the binary inputs of said plurality of inputs are divided according to a binary tree into inputs into a plurality of said logic units.

100. (Original) A logic circuit according to claim 99, wherein said logic units are arranged to receive 2^n of said binary inputs, where n is an integer indicating the level of the logic units in the binary tree, said logic circuit has m logic units at each level, where m is a rounded up integer determined from (the number of binary inputs)/ 2^n, logic units having a higher level in the binary tree comprise logic of logic units at lower levels in the binary tree, and each logic unit is arranged to generate logic unit binary outputs as a symmetric function of the binary inputs to the logic unit.

101. (Original) A logic circuit according to claim 100, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as a small elementary symmetric function of the binary inputs to said logic circuit.

102. (Original) A logic circuit according to claim 100, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit using OR logic for combining the binary inputs.

103. (Original) A logic circuit according to claim 102, wherein each logic unit at the first level is arranged to logically AND each of the binary inputs to the logic unit and to logically OR each of the binary inputs to the logic unit to generate the logic unit binary outputs.

104. (Original) A logic circuit according to claim 101, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit using exclusive OR logic for combining the binary inputs.

105. (Original) A logic circuit according to claim 104, wherein each logic unit at the first level is arranged to logically AND each of the binary inputs to the logic unit and to logically exclusively OR each of the binary inputs to the logic unit to generate the logic unit binary outputs.

106. (Original) A logic circuit according claim 100, wherein elementary logic units are provided as the logic units at the first level for performing elementary symmetric functions, outputs from each of two primary elementary logic units receiving four logically adjacent binary inputs from said plurality of inputs are input to two secondary elementary logic units, an output from each of the secondary elementary logic units is input to a tertiary elementary logic unit, and said primary, secondary and tertiary elementary logic units form a secondary logic unit at a second level of the binary tree having a binary output comprising a binary output from each of said secondary elementary logic units and two binary outputs from said tertiary elementary logic unit.

107. (Original) A logic circuit according to claim 106, wherein tertiary logic units at a third level of the binary tree each comprise two secondary logic units receiving eight logically adjacent binary inputs from said plurality of inputs, four elementary logic units receiving as inputs the outputs of said two secondary logic units, and further logic for generating binary outputs as a symmetric function of the binary inputs to said tertiary logic unit using the binary outputs of said four elementary logic units.

108. (Previously Presented) A logic circuit according to claim 107, wherein quaternary logic units at a fourth level of the binary tree each comprise two tertiary logic units receiving sixteen logically adjacent binary inputs from said plurality of inputs, four elementary logic units

receiving as inputs the outputs of said two tertiary logic units, and further logic for generating binary outputs as a symmetric function of the binary inputs to said quaternary logic unit using the binary outputs of said four elementary logic units.

109. (Original) A logic circuit according to claim 100, wherein elementary logic units are provided as the logic units at the first level for performing elementary symmetric functions, and logic units for higher levels are comprised of logic units of lower levels.

110. (Original) A logic circuit according to claim 109, wherein said logic units for higher levels above the second level comprise logic units of an immediately preceding level and elementary logic units.

111. (Original) A logic circuit according to claim 100, wherein each logic unit at each level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit using OR logic for combining the binary inputs.

112. (Original) A logic circuit according to claim 100, wherein each logic unit at each level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit using exclusive OR logic for combining the binary inputs.

113. (Original) A logic circuit according to claim 97, wherein the logic units are arranged hierarchically and at least one logic unit in at least one level of the hierarchy implements an inverted elementary symmetric function.

114. (Original) A logic circuit according to claim 113, wherein logic units at an odd number of levels in the hierarchy implement inverted elementary symmetric functions, logic units at an even number of levels in the hierarchy implement symmetric functions, and the inputs to the logic units at the first level of the hierarchy are inverted.

115. (Original) A logic circuit according to claim 113, wherein logic units at an even number of levels in the hierarchy implement inverted elementary symmetric functions, logic units at an even number of levels in the hierarchy implement symmetric functions, and the inputs to the logic units at the first level of the hierarchy are input to logic units in a first level in the hierarchy uninverted.

116. (Original) A logic circuit according to claim 113, wherein logic units at an even number of levels in the hierarchy implement inverted elementary symmetric functions, logic units at an odd number of levels in the hierarchy implement symmetric functions, and the inputs to the logic units at the first level of the hierarchy are inverted.

117. (Original) A logic circuit according to claim 113, wherein at least one logic unit in at least one level of the hierarchy implements an elementary symmetric function and the or each inverted elementary symmetric function and the or each elementary symmetric function are implemented in alternated levels in the hierarchy.

118. (Original) A logic circuit according to claim 113, wherein logic units in at least one level in the hierarchy comprise inversion logic.

119. (Original) A logic circuit according to claim 113, wherein the logic units are arranged hierarchically in a binary tree structure.

120. – 128. (Cancelled)

129. (Original) A computer system for designing a logic circuit comprising a plurality of inputs for receiving a binary number as a plurality of binary inputs, at least one output for outputting binary code, and logic elements connected between the plurality of inputs and the or each binary output and arranged to generate the or each binary output as a threshold function of the binary inputs, the computer system comprising:

a memory storing computer readable code;

a processor for reading and implementing the code;

wherein the code stored in the memory comprises code for controlling the processor to:

determine logic elements for performing the threshold functions; and

reduce the logic elements by identifying logic elements performing a logical AND of two threshold functions and reducing the identified logic elements to logic elements for performing the threshold function having the higher threshold, and identifying logic elements performing a logical OR of two threshold functions and reducing the identified logic elements to logic elements for performing the threshold function having the lower threshold.

130. (Original) A computer system according to claim 129, wherein the code stored in the memory comprises code for controlling the processor to: perform the reduction using logical OR threshold functions having the relationship:

$$OR\_n\_k \wedge OR\_n\_s = OR\_n\_k$$

$$OR\_n\_k \vee OR\_n\_s = OR\_n\_s$$

where $k \geq s$, n is the number of inputs and k and s are the number of high inputs.

131. (Original) A computer system according to claim 129, wherein the code stored in the memory comprises code for controlling the processor to: design the logic elements to perform the threshold functions as elementary symmetric functions, and to generate the or each binary output as an elementary symmetric function.

132. – 138. (Cancelled)

139. (Original) A computer system for designing a logic circuit comprising a plurality of inputs for receiving a binary number as a plurality of binary inputs, a plurality of outputs for outputting binary code, and logic elements connected between the plurality of inputs and the binary outputs and arranged to generate each binary output as a symmetric function of the binary inputs, the system comprising:

a memory storing computer readable code;

a processor for reading and implementing the code;

wherein the code stored in the memory comprises code for controlling the processor to:

design the logic circuit using exclusive OR logic;

identify any logic which cannot have inputs that are high at the same time; and

replace the identified exclusive OR logic with OR logic.

140. (Original) A computer system according to claim 139, wherein the code stored in the memory comprises code for controlling the processor to design the logic circuit to generate each binary output as an elementary symmetric function of the binary inputs.

141. (Original) A computer system according to claim 139, wherein the code stored in the memory comprises code for controlling the processor to design the logic circuit as a parallel counter having a plurality of outputs.

142. – 144. (Canceled)

145. (Original) A system for designing a logic circuit comprising:

storing means storing a library of logic module designs each for performing a small symmetric function;

designing means for designing a logic circuit to perform a large symmetric function; identifying small symmetric functions which can perform said symmetric function;

first selecting means for selecting logic modules from said library to perform said small symmetric functions;

identifying means for identifying a logic circuit in the selected logic circuit which performs a symmetric function and which can be used to perform another symmetric function; and

second selecting means for selecting the logic circuit corresponding to the identified symmetric function and using the selected logic circuit with inverters to perform said other symmetric function using the relationship between the symmetric functions:

$$OR\_n\_k(X_1...X_n) = \neg OR\_n\_(n+1-k)(\neg X_1...\neg X_n)$$

where ¬ denotes an inversion, n is the number of inputs, and k is the number of sets of inputs AND combined together.

146. (Original) A system according to claim 145, wherein the symmetric functions are elementary symmetric functions.

147. (Original) A computer system for designing a logic circuit comprising:

a data memory storing a library of logic module designs each for performing a small symmetric function;

a code memory storing computer readable code;

a processor for reading and implementing the code;

wherein the code stored in the code memory comprises code for controlling the processor to:

design a logic circuit to perform a large symmetric function;

identifying small symmetric functions which can perform said symmetric function;

select logic modules from said library to perform said small symmetric functions;

identify a logic circuit in the selected logic circuit which performs a symmetric function and which can be used to perform another symmetric function; and

select the logic circuit corresponding to the identified symmetric function and using the selected logic circuit with inverters to perform said other symmetric function using the relationship between the symmetric functions:

$$OR\_n\_k(X_1...X_n) = \neg OR\_n\_(n+1-k)(\neg X_1...\neg X_n)$$

where ¬ denotes an inversion, n is the number of inputs, and k is the number of sets of inputs AND combined together.

148. (Original) A computer system according to claim 147, wherein the symmetric functions are elementary symmetric functions.

149. (Cancelled)

150. (Previously Presented) A parallel counter according to claim 43, wherein said logic circuit is arranged to generate at least two outputs independently of each other.

151. (Previously Presented) A parallel counter according to claim 43, wherein said logic circuit is arranged to generate at least one of the binary outputs as an elementary symmetric function of the binary inputs using exclusive OR logic for combining a plurality of sets of one or more binary inputs.

152. (Previously Presented) A parallel counter according to claim 151, wherein said logic circuit is arranged to logically AND members of each set of binary inputs and to logically exclusively OR the result of the AND operations.

153. (Previously Presented) A parallel counter according to claim 152, wherein said logic circuit is arranged to logically AND 2^i of the binary inputs in each set for the generation of the i^{th} binary output, where i is an integer from 1 to N, N is the number of binary outputs and i represents the significance of each binary output, each set being unique and the sets covering all possible combinations of binary inputs.

154. (Previously Presented) A parallel counter according to claim 152, wherein said logic circuit is arranged to logically AND members of each set of binary inputs, where each set is unique and the sets cover all possible combinations of binary inputs.

155. (Previously Presented) A parallel counter according to claim 43, wherein said logic circuit is arranged to generate at least one of the binary outputs as an elementary symmetric function of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs.

156. (Previously Presented) A parallel counter according to claim 155, wherein said logic circuit is arranged to logically AND members of each set of binary inputs and to logically OR the result of the AND operations.

157. (Previously Presented) A parallel counter according to claim 156, wherein said logic circuit is arranged to logically AND 2^{N-1} of the binary inputs in each set for the generation of the N^{th} binary output, where N is the number of binary outputs and the N^{th} binary output is the most significant, each set being unique and the sets covering all possible combinations of binary inputs.

158. (Previously Presented) A parallel counter according to claim 157, wherein said logic circuit is arranged to logically AND members of each set of binary inputs, where each set is unique and the sets cover all possible combinations of binary inputs.